



KOREAN PATENT ABSTRACTS(KR)

Document Code:A

(11) Publication No.1020030059437 (43) Publication.Date. 20030710

(21) Application No.1020010088298 (22) Application Date. 20011229

(51) IPC Code:

H01L 21/76

(71) Applicant:

HYNIX SEMICONDUCTOR INC.

(72) Inventor:

JUN, SEUNG JUN

(30) Priority:

(54) Title of Invention

METHOD FOR FORMING ISOLATION LAYER OF SEMICONDUCTOR DEVICE

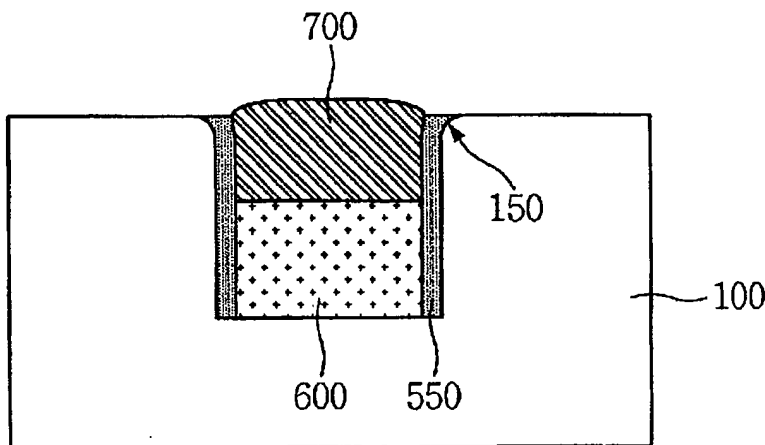
Representative drawing

(57) Abstract:

PURPOSE: A method for forming an isolation layer of a semiconductor device is provided to be capable of reducing junction leakage current and maintaining constantly breakdown voltage by filling a trench using SEG(Selective Epitaxial Growth).

CONSTITUTION: After sequentially forming a buffer oxide layer and a nitride layer on a semiconductor substrate(100), a trench is formed in the substrate. An under-cut is formed by selectively etching the buffer oxide layer. After rounding the top edges of the trench using hydrogen annealing, an oxide layer(150) is formed to fill the under-cut. An oxide spacer(550) is formed at inner walls of the trench by selectively etching the oxide layer. A silicon layer(600) is partially filled in the trench by using SEG. A gap-fill oxide layer(700) is entirely filled into the trench.

© KIPO 2003



if display of image is failed, press (F5)